ABSTRACT OF THE DISCLOSURE

Methods of manufacturing a semiconductor integrated circuit using selective disposable spacer technology and semiconductor integrated circuits manufactured thereby: The method includes forming a plurality of gate patterns on a semiconductor substrate. Gap regions between the gate patterns include first spaces having a first width and second spaces having a second width greater than the first width. Spacers are formed on sidewalls of the second spaces, and spacer layer patterns filling the first spaces are also formed together with the spacers. The spacers are selectively removed to expose the sidewalls of the first spaces. As a result, the semiconductor integrated circuit includes wide spaces enlarged by the removal of the spacers and narrow and deep spaces filled with the spacer layer patterns.